Listing and Amendments to the Claims

This listing of claims will replace the claims that were published in the PCT Application:

1. (currently amended) Physical layer circuit for an interface circuit to a first communication bus ~~(7)~~, the physical layer circuit comprising a buffer memory ~~(22)~~ for node-ID packets received via a bridge circuit from a second communication bus ~~(8)~~, ~~characterised in that~~ wherein the physical layer circuit ~~(21)~~ comprises configuration means ~~(24)~~ that enable to either configure the physical layer circuit ~~(21)~~ as a bridge portal physical layer circuit supporting the bridge functionality by buffering said node-ID packets in said buffer memory ~~(22)~~ or else configure the physical layer circuit as a standard physical layer circuit not supporting bridge functionality by disabling the buffering of said node-ID packets.

2. (currently amended) Physical layer circuit according to claim 1, the configuration means ~~(24)~~ comprising a configuration register having one or more register places dedicated to the enabling or disabling of the node-ID packet buffering.

3. (original) Physical layer circuit according to claim 2, wherein the configuration register is a read/write register.

4. (currently amended) Physical layer circuit according to claim 2 ~~or 3~~, wherein a pin ~~(CON)~~ of the physical layer circuit ~~(21)~~ is connected with the register place dedicated to the enabling or disabling of the node-ID packet buffering.

5. (currently amended) Physical layer circuit according to claim 4, wherein the pin ~~(CON)~~ of the physical layer circuit is positioned at a place where a standard physical layer circuit not supporting the bridge functionality has a power supply pin, namely ground pin ~~(AGND)~~ or voltage supply pin ~~(AV_{DD})~~.

6. (currently amended) Physical layer circuit according to ~~one of the previous claims~~ claim 1, wherein the first and second communication bus ~~(7, 8)~~ is an IEEE1394 bus and the bridge ~~(9)~~ is a wireless bridge that performs wireless communication according to the Hiperlan/2 standard.

7. (currently amended) Physical layer circuit according to ~~one of the previous claims~~ claim 1, comprising a number of n ports ~~(23)~~ for the first communication bus ~~(7)~~, $n \in [2,3, \ldots]$.

8. (currently amended) Interface device for a first communication bus ~~(7)~~ comprising a physical layer circuit ~~(21)~~ according to claim 7, wherein said physical layer circuit ~~(21)~~ is configured as a bridge portal physical layer circuit with the buffering of node-ID packets being enabled, ~~characterised in that~~ wherein at maximum n-1 of the ports ~~(23)~~ for the first communication bus ~~(7)~~ are connected to corresponding sockets for bus cable plug insertion.